IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR PATENT

PROCESS TO IMPROVE HIGH PERFORMANCE CAPACITOR PROPERTIES IN INTEGRATED MOS TECHNOLOGY

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Background of the Invention

This invention relates to the fabrication of semiconductor devices as it applies to integrated circuits, and more specifically, to methods for the fabrication of capacitors in such a process.

As the scale of integrated circuits has decreased, a number of new techniques have been introduced to the manufacturing process. One of these is the use of Anti-Reflective Layers (ARLs). These include both grown or deposited varieties, such as Titanium Nitride or a Plasma Enhanced chemical vapor deposition Anti-Reflective Layer (PEARL), and coatings, such as an Anti-Reflective Coating (ARC).

The purpose of the ARL is to reduce net linewidth variations in the photolithographic process. Variations that are allowable within a 1μm or even 0.6μm process become unacceptable as devices move deeper into the submicron range: A variation of, say, ±0.1μm or even ±0.15μm in Critical Dimension (CD) may be tolerable at 1μm, but would produce a factor of 2 or 3 difference between the upper and lower values at the 0.3μm scale. Such variations in transistor gate length can undermine device performance and reliability, particularly on the low side. An ARL layer can readily reduce such variations in CD width by a third when compared to the same process without this layer.

The ARL is an additional step included as part of the photolithographic process. It is a highly absorbing film formed directly on the

substrate and upon which the photoresist then is formed. The ARL absorbs most of the radiation that penetrates the resist, generally in the 70-85% range. Standing waves are thereby substantially reduced as there is less reflection off the substrate and scattering from topological features is also suppressed. In addition, as an ARL partially planarizes the wafer topology, resist thickness is more uniform and linewidth variation over steps is improved.

This effect is shown in Figure 1, where CD in units of μm is plotted against resist thickness in units of Angstroms. The shown data points are for a set of reference structures formed to measure variations in critical dimension. The lower line, with data points indicated by a series of ×s, corresponds to a series of dense features without the use of an ARL. This curve is very sensitive to variations in resist thickness and shows a periodic structure due to standing waves.

The top three lines show the use of an ARL. The line formed on the solid squares corresponds to the same dense features as the non-ARL line of ×s and may be compared directly. The ARL line varies in a much smoother fashion than the non-ARL curve and is therefore far less sensitive to processing variations. The line of open triangles, corresponding to isolated features with the same structure as solid squares, and the line of solid circles, corresponding to a different structure, also show the uniformity produced by using an anti-reflective layer.

As is often the case with process technology, the solution to one problem often creates a new problem, or, in this case, causes a latent problem to manifest itself. The particular problem here is the ability to integrate a high performance capacitor into a standard CMOS process flow, where capacitor performance is defined in terms of stability over a wide voltage range and low leakage levels.

A more or less standard embodiment of a portion of this process flow can be given by the following series of steps:

Standard Transistor Flow

1. Lower electrode deposition
2. Lower electrode doping
3. Lower electrode anneal

Capacitor Process Module

4. Capacitor dielectric deposition
5. Upper electrode deposition
6. Upper electrode implant
7. Upper electrode anneal
8. Photo mask to define upper electrode
9. Upper electrode etch
10. Capacitor dielectric removal

Standard Transistor Flow continued

11. ARL formation
12. Photo mask to define lower electrode
13. Lower electrode etch
14. Poly oxidation for transistor and subsequent steps,

where the subsequent steps would include the standard fabrication steps, such as masking and implantation to form the transistors' source and drain, as well as any common but optional steps, such as, say, the formation of a Lightly Doped Drain (LDD). Some of the steps on this list are themselves optional but common, such as the anneal of steps 3 and 7 or, what is more pertinent here, step 11.

This list of steps is broken into three parts. Steps 1-3 are common to both the formation of transistors for the device as well as the capacitors. If the capacitors were not needed, the process would proceed directly from step 3 to step 11 for the ARL to be applied and steps 4-10 eliminated. The inclusion of steps 4-10 allows the fabrication of a high performance capacitor to integrated into this standard CMOS process flow. In this way, these steps can be added as a group, or module, when the device being fabricated requires capacitors and otherwise deleted without changing the non-capacitor, transistor steps or flow. A variation could define and etch the lower electrode before the capacitor dielectric is formed, but it

is preferred to integrate this with the etch of the standard transistor flow, particularly at 0.35μm and below.

Step 4 forms a dielectric for the capacitors, such as an oxide, an Oxide-Nitride-Oxide (ONO) sandwich, oxynitride, or one of the other standard variations. Steps 5-9 form the upper electrodes, the lower electrodes having been formed, but not defined, at the same time as those for the transistors in steps 1-3. This leaves the capacitor dielectric at the end of step 9. This dielectric could be left at this stage and step 10 eliminated, its removal being incorporated into step 13 when the lower electrodes are etched. This would, however, require a revision of steps 12 and 13 as having this extra layer still on the substrate would change the reflectivity of the stack. The various settings for all the process parameters would then need to be recalibrated accordingly. Aside from the practical difficulties and complexities this would introduce, it would also mean that steps 4-10 were no longer an independent "module" which could be inserted or deleted depending on device requirements. For this reason, step 10 is included for ease of integration into the standard CMOS process.

Step 11 follows and is included for the reasons described earlier. It is an optional step and introduces an added layer of complexity to the process. For this reason it is normally omitted for device near or above the micron level, but is increasingly standard as devices move ever deeper into the submicron range.

The problem in this process as found in the prior is in the juxtaposition of step 10 with step 11: It is this combination of the dielectric removal with the application of an anti-reflective layer having poor insulation properties that is detrimental to the capacitors.

This problem is that step 10 not only removes the unwanted capacitor dielectric, but will also undercut into the wanted portion below the upper electrode. This situation is shown in Figure 3, which represents the process through step 10. This shows the undefined lower electrode layer 120 upon the field oxide or other underlying layers 130 included to electrically isolate it. The upper electrode 140 has been defined and etched, and is separated from the lower electrode 120 by the

dielectric layer 160. Ideally, the dielectric 160 would have its sides even with those of the upper electrode. Instead, it suffers from the undercutting indicated at 180.

If processing were to continue as is common for a 1μm or even 0.6μm, namely, without the ARL of step 11, this would not cause any major problems. In this case, steps 12 and 13 define and etch the lower electrode immediately after step 10; and are themselves followed by the formation of the transistor oxide in step 14. At this point, again with step 11 absent, this undercutting will have been filled back in by a non-conductor such as BPSG, a silicate glass, and degradation of the capacitors' dielectric will be minimal or non-existent.

This is demonstrated in Figures 10 and 11, where the solid diamonds represent this process without the ARL of step 11. Figure 10 shows cumulative probability vs. capacitor leakage current at 5 volts, with the horizontal scale logarithmic in units of $fA/\mu m^2$. For the process without an anti-reflective layer, this is a nearly vertical line at a value of $10^{-1.5} \approx 0.03 fA/\mu m^2$. Figure 11 is a plot of cumulative probability vs. capacitor voltage coefficient. This is a measure of capacitance as a function of the voltage across its plates: For an idealized conducting electrode capacitor, capacitance is independent of voltage and the graph would be a vertical line at 0. For a capacitor formed on a semiconductor device, the plates of the capacitor are now of doped silicon or similar material and the deviation from this ideal is measured in PPM per volt. The line should still be as vertical as possible, for device consistency, and as close to zero as possible, for the best performance of the individual capacitors. The solid diamonds of the non-ARL process are again nearly vertical and with a magnitude of just over 20PPM/V, the negative values a residue of how the coefficient is defined. This set of points, the solid diamonds, can be seen as reference values against which a fully integrated process can be measured.

With the inclusion of both steps 10 and 11, this undercutting is now filled in by the less benign ARL. In particular, PEARL is a silicon rich Si_xON_y film and is expected to be a poor insulator, resulting in high leakage currents. This will greatly degrade both device performance, due to leakage well beyond design

specifications, and stability, as variations in performance will vary over a wide voltage range of values as the amount undercutting will vary from capacitor to capacitor. This is shown on Figures 10 and 11 by the solid squares. In Figure 10, these points are well to the right of the reference values with leakage currents of, at best, several orders of magnitude higher. In Figure 11, these points are far from vertical, showing a capacitance that is very voltage dependent due to excessive leakage.

Even when the undercutting, 180 of Figure 3, is minimized or eliminated by using, say, a dry etch in step 10, the combination of step 10 with step 11 can still cause capacitor degradation. Although the ARL no longer intrudes significantly into the inter-electrode region, its proximity still affects performance if the ARL is not sufficiently insulating, as is the case for PEARL.

Therefore, it is an objective of the present invention to integrate a high performance capacitor into a CMOS process flow, particularly where the flow incorporates an anti-reflective layer to reduce variations in critical dimension width.

Summary of the Present Invention

These and additional objects are accomplished by the various aspects of the present invention, wherein, briefly and generally, a method of fabricating a high performance capacitor that may be incorporated into a standard CMOS fabrication process suitable for submicron devices. The parameters used in the standard CMOS process may be maintained, particularly for the definition and etch of the lower electrode layer that also serves as the transistor gate. To reduce variation in critical dimension width, an Anti-Reflective Layer (ARL) is used. In the preferred embodiment, this is of the Plasma Enhanced chemical vapor deposition Anti-Reflective Layer (PEARL) type, although other Anti-Reflective Coatings (ARCs) or layers, such as a conductive film like titanium nitride (TiN), may be used. This ARL formation occurs after the capacitor specific process steps, but prior to the masking used for defining the lower electrodes.

In one embodiment, a Rapid Thermal Oxidation (RTO) is performed subsequent to removing the unwanted capacitor dielectric layer from the transistor poly outside of the capacitor regions, but prior to the PEARL deposition. This RTO is thin enough to not require a reformulation, due to changes in reflectivity, of the later process steps used in forming the transistors and other subsequent devices, yet thick enough to alleviate the degradation of capacitor performance due to the PEARL filling in any undercutting that occurred when the capacitor dielectric layer was removed. This is found to produce capacitors with low leakage and stability over a wide voltage range, with values comparable to those obtained with the PEARL absent.

Another embodiment instead eliminates the capacitor dielectric removal step. It is then replaced by a step to form an additional layer which, in a second step, is then etched away to leave spacers on the capacitor sides, thereby eliminating any undercutting of the dielectric. These new steps are both prior to the ARL formation and, as with the other embodiment, improve capacitor performance.

A further embodiment also eliminates the capacitor dielectric layer removal step prior to the ARL formation and forms the ARL on the dielectric and upper capacitor electrodes. The dielectric is then removed at the same time as the lower capacitor electrodes and transistor gates are formed.

Additional objects, advantages, and features of the present invention will become apparent ~~form~~ from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Figure 1 shows variations in critical dimension with resist thickness with and without an anti-reflective layer.

Figure 2 shows an embodiment of the present invention at the stage where the upper electrode has been defined.

Figure 3 shows the same embodiment after the excess capacitor dielectric has been removed.

Figure 4 again shows the same embodiment of the present invention after forming a thin insulating layer.

Figure 5 is a later stage of the same embodiment where an ARL has been applied.

Figure 6 is the same as Figure 2, but as the precursor to an alternate embodiment.

Figure 7 shows the alternate embodiment after a capacitor spacer layer has been formed.

Figure 8 is Figure 7 subsequent to etching.

Figure 9 is the alternate embodiment after an ARL has been applied.

Figure 10 shows cumulative probability plot for capacitor leakage of different embodiments.

Figure 11 shows cumulative probability plot for capacitor voltage coefficient of different embodiments.

Description of the Preferred Embodiment

A primary objective of the present invention is to present a process for the integration of a high performance capacitor into a standard CMOS fabrication process flow. In this context, high performance is defined to consist of low leakage levels and stability over a wide voltage range as would be required to achieve a 12 bit or higher analog to digital conversion capability. It is preferred that the steps required to form these capacitors should not require any change in the process parameters for the non-capacitor stages. The preferred application of the described methods is in the submicron range, particularly on the order of 0.35μm or below, where Anti-Reflective Layers (ARLs) are used to reduce variations in critical dimension width. The preferred ARLs are of the Plasma Enhanced chemical vapor deposition Anti-Reflective Layer (PEARL) variety, although others may be substituted, such as TiN. This invention is also applicable for any non-insulating and/or low dielectric strength layer placed on both electrodes of a capacitor after dielectric removal.

A preferred embodiment of the present invention is given by the series of steps:

Standard Submicron Core Technology Flow

1. Lower electrode formation
2. Lower electrode doping
3. Lower electrode anneal

Capacitor Process Module

4. Capacitor dielectric formation
5. Upper electrode formation
6. Upper electrode doping
7. Upper electrode anneal
8. Photo mask to define upper electrode
9. Upper electrode etch
10. Capacitor dielectric removal

10a. RTO

Standard Submicron Core Technology Flow continued

11. ARL/PEARL formation.
12. Photo mask to define lower electrode
13. Lower electrode etch
14. Poly oxidation for transistor and subsequent steps,

where steps 9-11 are shown in Figures 2-5. Steps 1-3 and steps 11 on are part of the transistor fabrication process, while steps 4-10a are specific to capacitor formation. These steps differ from the more or less generic prior art by the inclusion of step 10a. The next few paragraphs describe the details of these steps according to this preferred embodiment.

Taking up the process at the formation of the lower electrodes, steps 1-3 are part of the standard transistor formation flow and are common for both the capacitors and later transistor formation steps. In step 1, the layer to serve as lower electrodes and the transistor gates is formed, preferably of amorphous silicon with a thickness of 2000Å to 4000Å. This layer is then doped in step 2, preferably implanted using phosphorus dose levels of from $5\times10^{15}cm^{-2}$ to $2\times10^{16}cm^{-2}$, although this could also be done in a non-implant method such as with $POCl_3$. This is

followed by the optional but common step of an anneal, preferably by Rapid Thermal Processing (RTP), with a furnace anneal as another possibility.

At this stage, the steps specific to capacitor formation occur. A capacitor dielectric is formed in step 4, deposited or grown to a thickness in the range of 300Å to 800Å. Upon this dielectric the upper electrode is formed, doped, and annealed in steps 5-7. In the preferred embodiment, this is amorphous silicon with a thickness in the range of 1500Å to 2500Å, which has again been implanted by phosphorus, now with a dose in the $0.5\text{-}1.5\times10^{16}cm^{-2}$ range, and subjected to an RTP anneal. Alternate embodiments could use other conductors such as TiN or tungsten for the electrode or, as with the lower electrode, other doping and annealing techniques. The upper electrode is then masked and etched in steps 9 and 10, leaving the structure shown in Figure 2.

The right hand side of Figure 2 corresponds to the capacitor sector and shows the defined upper electrode 140 on the capacitor dielectric 160, which is in turn on the lower electrode 120. The left hand side of Figure 2, and Figures 3-9, correspond to the transistor sector of the device at the same stage as the capacitor sector on the right. At this stage the dielectric layer 160 has not been etched and the lower electrode is doped but undefined. The field oxide or other underlying layers 130 are included to electrically isolate the lower electrode/transistor gate layer 120.

Step 10 is the etch of the capacitor dielectric. In the preferred embodiment, this is a Buffered Oxide Etch (BOE), although other embodiments could employ a dry or other etch. Still another embodiment could completely dispense with this etch, but as discussed below, this would complicate the integration of the capacitor process steps into the larger process due to transistor gate length variation.

The result of this process is shown in Figure 3. In this figure, the unwanted portions of the dielectric layer 160 have been removed in preparation for the PEARL deposition. An unwanted consequence of step 10 is that, as discussed in the background section, some of the wanted dielectric is also removed. This is the undercutting indicated in Figure 3 at 180.

The preferred application of these embodiments is in a 0.35μm mixed mode technology, where the specified length variation of the transistor gates formed from layer 120 in step 13, ΔL_{eff}, is ± 0.05μm. The inclusion of the ARL allows for these tolerances, which otherwise would likely exceed ± 0.15μm. Since the PEARL is a silicon rich Si_xON_y film, it has poor insulating properties and needs to be kept from between the capacitor plates or from contacting both of them. The specified performance for the capacitors is less than 4fA/μm^2 of leakage current and less than 50 PPM/V for the voltage coefficient, suitable for the 14 bit analog resolution of the device employing this technique as the preferred embodiment. The inclusion of step 10a provides electrical insulation and makes this possible.

Another option would be to leave the entire capacitor dielectric layer 160 on the lower electrode and to deposit the PEARL or other ARL onto the capacitor dielectric rather than directly on the underlying layer 130; that is, eliminate step 10 and do not introduce step 10a. Steps 12 and 13 would then define and etch the dielectric along with the lower electrode. This process corresponds to the open squares of Figures 10 and 11 and, as discussed below, shows performance similar to when no PEARL layer is used. Thus, this option allows for the incorporation of a PEARL layer while maintaining capacitor performance: However, this would not allow the capacitor formation subprocess to be integrated into the fabrication process without a modification of process parameters and the consequent reformulation difficulties, as well as adding variation to the manufacturing steps required. For example, using the values of preferred embodiment, the transistor gate photolithographic process would need to be optimized, as the preferred non-capacitor process PEARL thickness of approximately 375Å is insufficient to achieve the preferred L_{eff} variation with an dielectric layer of approximately 375Å underneath. To match the described process of 375Å PEARL with no dielectric would require something on the order of 800Å PEARL if the 375Å dielectric layer were left in place. Such reparameterizations result in other process difficulties that would require resolution and necessitate two different process recipes, one for capacitors and one without capacitors.

Returning to the process flow of the preferred embodiment, in step 10a the structure of Figure 3 is subjected to a Rapid Thermal Oxidation (RTO). This involves a short oxidation in an RTO tool to grow to a layer of oxide, preferably 20Å to 60Å thick, although this could be increased to 70Å or 100Å if the extra thickness did not produce excessive degradation of the photolithographic process. This is performed for 10s to 60s at a temperature of from 850°C to 1050°C, with values in the lower part of the range preferred for minimal impact on transistor performance. The result is shown in Figure 4, where the rapid thermal oxide 170 has sealed in the previous structure by filling in the undercut between the capacitor plates 140 and 120. The RTO layer is left on the lower electrode during the PEARL deposition. The chosen thickness for the RTO layer is a compromise: It needs to be thick enough to fill in the undercut 180, yet thin enough to not significantly degrade a photolithographic process, particularly in the transistor sector, based on previously determined parameters. At 20Å to 60Å, this is roughly an order of magnitude thinner than removed capacitor dielectric 160 and the original setting may still be successfully employed. In other embodiments, this oxide or other dielectric could be formed in a furnace or possibly even deposited with an optional anneal.

Figure 5 shows the PEARL 190 as deposited in step 11. In the preferred embodiment this layer is 300Å to 400Å. At this stage, the standard transistor process flow continues, with steps 12 and 13 defining and etching the lower electrodes, including those of the capacitors as well as the transistor gates.

An alternate embodiment is shown in Figures 6-9 and follows the following series of steps:

Standard Submicron Core Technology Flow

1. Lower electrode formation
2. Lower electrode doping
3. Lower electrode anneal

Capacitor Process Module

4. Capacitor dielectric formation
5. Upper electrode formation
6. Upper electrode doping
7. Upper electrode anneal
8. Photo mask to define upper electrode
9. Upper electrode etch

(delete 10. Capacitor oxide removal)

10'. Spacer oxide deposition or growth
10". Capacitor dielectric and spacer etch

Standard Submicron Core Technology Flow continued

11. ARL/PEARL formation
12. Photo mask to define lower electrode
13. Lower electrode etch
14. Poly oxidation for transistor and subsequent steps.

Steps 1-9 of this embodiment are the same as in the previously described embodiment. The preferred values of the parameters are also the same. This is also true from step 11 onward. The difference is in the deletion of step 10 and, instead of including step 10a, the inclusion steps 10' and 10".

The purpose and effect of steps 10' and 10" is the same as step 10a above, namely to further remove the poorly insulating ARL into the interelectrode region of the capacitor. In this alternate embodiment this is done by preventing this gap from forming, while in the previous embodiment this gap was allowed to form, but subsequently refilled and the PEARL was then electrically isolated.

Figure 6 shows the situation at the end of step 9 and is therefore the same as Figure 2. In step 10' a capacitor spacer insulating layer 175 is formed on this structure as shown in Figure 7. This insulating layer is preferably oxide and may be grown or, preferably, deposited to a thickness of 500Å to 2000Å in the preferred embodiment of this variation.

In step 10", both this spacer oxide 175 and the original capacitor dielectric 160 are etched back to the lower electrode 120. The resultant structure is shown in Figure 8. Instead of the undercutting found in Figure 3, a spacer 185, preferably with a thickness of 500Å to 2000Å, now remains on either side of the

capacitor. This is composed of the combination of the oxide layer 175 and dielectric layer 160. In this manner, the interpoly portions of dielectric 160 is protected so that the PEARL may not infiltrate into this region while at the same time the dielectric layers 175 and 160 are no longer in the transistor sector.

Figure 9 shows the result of step 11 in this embodiment after the PEARL deposition. The remaining process steps are now the same as in the previously described embodiment or, equivalently at this stage, the standard non-capacitor flow.

Either of these embodiments substantially improves the performance of the capacitors, as shown in Figure 10 and 11. Figure 10 shows cumulative probability vs. capacitor dielectric leakage current at 5 volts, where the horizontal scale is logarithmic in units of $fA/\mu m^2$, and Figure 11 is a plot of cumulative probability vs. capacitor voltage coefficient PPM/volt. The graph has five series of points: the circles correspond to the described embodiments, the open circle the preferred embodiment using the RTO process of step 10a and the solid circle the alternative embodiment with the spacer of steps 10' and 10".

As described in the background section, the solid squares correspond to the prior art while the solid diamonds are for reference and correspond to the desired result. ~~These last show leakage levels when the capacitor layer is etched and the problematical PEARL level is absent, corresponding to the process through step 10, and produce near vertical lines at a value of approximately $10^{-1.5} \approx 0.03 fA/\mu m^2$, well below the design objective.~~ As discussed in the background section, this process is not preferred since the PEARL layer used in the deep submicron region is lacking. The values for the prior art (solid squares) lie well to the right of these reference values. This is a consequence of the degradation of the interpoly dielectric from the PEARL. Even when undercutting of the capacitor dielectric, indicated at 180 in Figure 3, is small, if the ARL has poor insulating properties, such as for the preferred PEARL layer, leakage between upper and lower electrodes can occur. The preferred embodiment (open circles) differs very little ~~form~~ from the reference values, producing a quite vertical lines at nearly the same values in both Figures 10 and 11.

The alternative embodiment's values (closed circles) do not coincide as well, but still show improvement compared to the prior art.

The open squares show the process omitting step 10 and removing the dielectric as part of the lower electrode etch. This alternative embodiment mentioned above corresponds to leaving the capacitor dielectric on the lower electrode and to depositing the ARL onto the dielectric rather than directly on the underlying layer. The results for this method are very close to those where the ARL is missing, with the points of the open squares nearly coinciding with those of the solid diamonds. Thus, one way to still maintain capacitor performance would be to omit step 10 without including any additional steps. However, as discussed above, this option would not allow the capacitor formation subprocess to be integrated into the fabrication process without a modification of process parameters and the consequent reformulation difficulties, as well as adding variation to the manufacturing steps required. The capacitor process module of steps 4-10 could no longer be included or excluded as needed without also altering the other portions of the process, particularly steps 11, 12, and 13 which immediately follow. However, for applications that do not require the capacitor formation process to be integrated into a CMOS process, or that would allow the initial parameter formulation based upon it, this alternative embodiment would then become the preferred embodiment.

Finally, it should be noted that although this discussion has been in terms of an integrated capacitor/CMOS process flow using ARLs, the invention is of wider applicability. The focus here has been on ARLs due to their increasing importance, but a process using another poorly insulating layer at the corresponding process step would similarly benefit. Similarly, whether involving an ARL or other non-insulator, these techniques could improve capacitor production even when not integrated into a CMOS process, particularly those of the embodiment of the previous paragraph.

Various details of the implementation and method are merely illustrative of the invention. It will be understood that various changes in such

details may be within the scope of the invention, which is to be limited only by the appended claims.